AMENDMENTS TO THE CLAIMS:

Claim 1. (Currently Amended) A semiconductor device comprising:

a first MOSFET ~~designed to have a threshold level which is relatively lower, the first MOSFET~~ having a first gate oxide film;

a second MOSFET ~~of an n-type designed to have a threshold level which is relatively higher, the second MOSFET~~ having a second gate oxide film thicker than the first gate oxide film; and

a third MOSFET of a p-type ~~designed to have a threshold level which is relatively higher than said first MOSFET, the third MOSFET~~ having a third gate oxide film which is thicker than the first gate oxide film and is thinner than the second gate oxide film, wherein said second MOSFET and said third MOSFET form a single CMOS pair.

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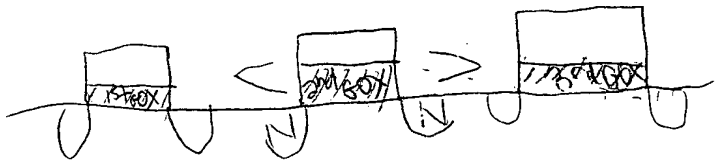
Claim 2. (Previously canceled)



Claim 3. (Previously amended - withdrawn) A method for fabricating on a semiconductor substrate a semiconductor device, the method comprising:

forming an isolation region within a semiconductor substrate and close to a surface of the semiconductor substrate to define a first region for a first gate oxide film of a first MOSFET and a second region for second and third MOSFETs;

selectively implanting fluorine ions into a first part of the second region with a first ion-implantation condition, the first part of the second region being for the second MOSFET, the first ion-implantation condition being determined to form a second gate oxide film;

selectively implanting fluorine ions into a second part of the second region with a

second ion-implantation condition, the second part of the second region being for the third MOSFET, the second ion-implantation condition being determined to form a third gate oxide film;

simultaneously growing oxide films on and over the first and second regions of the semiconductor substrate; and

forming the first to third MOSFETs by using the simultaneously grown oxide films, so that the first to third MOSFETs have the first to third gate oxide films, respectively, wherein the second gate oxide film is thicker than the first gate oxide film and the third gate oxide film is thicker than the first gate oxide film and is thinner than the second gate oxide film; and

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wherein the threshold level of the first MOSFET is relatively low and the threshold levels of the second and third MOSFETs are relatively high, and the second MOSFET is an n-type and the third MOSFET is a p-type, wherein said second MOSFET and said third MOSFET form a single CMOS pair.

4. (Previously amended - withdrawn) A fabrication method as claimed in claim 3, wherein the first and second ion-implantation conditions are determined so that the third gate oxide film is thinner than the second gate oxide film.

5. (Previously presented - withdrawn) A fabricating method as claimed in claim 4, wherein the first ion-implantation condition comprises first dosage of fluorine ions and predetermined implantation energy, while the second ion-implantation condition comprises second dosage of fluorine ions and the predetermined implantation energy, the second dosage

being less than the first dosage.

6. (Previously presented - withdrawn) A fabricating method as claimed in claim 5, wherein the first dosage is of 7.0 $\sim 10^{14}$-1.2 $\sim 10^{15}/cm^2$ inclusive, and the predetermined implantation energy is 5keV.

7. (Previously presented - withdrawn) A fabricating method as claimed in claim 6, wherein the second dosage is equal to or below 6.0 $\sim 10^{14}/cm^2$.

8. (Previously presented - withdrawn) A fabricating method as claimed in claim 4, wherein the first ion-implantation condition comprises predetermined dosage of fluorine ions and first implantation energy, while the second ion-implantation condition comprises the predetermined dosage of fluorine ions and second implantation energy, the second implantation energy being higher than the first implantation energy.

9. (Previously presented - withdrawn) A fabricating method as claimed in claim 8, wherein the predetermined dosage is 6.0 $\sim 10^{14}/cm^2$, and the first and second implantation energies are 3keV and 5keV, respectively.

10. (Previously presented - withdrawn) A fabricating method as claimed in claim 4, wherein the first and second ion-implantation conditions are further determined so that the second and third MOSFETs have gate-channel leakage current characteristics substantially equal to each other.

11. (Previously presented - withdrawn) A fabricating method as claimed in claim 10, wherein the first and second ion-implantation conditions are further determined so that standby current in the second and third MOSFETs do not depend on the gate-channel leakage current characteristics but on subthreshold characteristics of the second and third MOSFETs.

12. (Previously presented - withdrawn) A fabricating method as claimed in claim 3, further comprising:

before the selectively implanting fluorine ions into the first part of the second region, forming P-well as the first part within the second region; and

before the selectively implanting fluorine ions into the second part of the second region, forming N-well as the second part within the second region.

13. (Previously presented - withdrawn) A fabricating method as claimed in claim 12, wherein the forming P-well is carried out by selectively implanting boron ions into a part of the second region that becomes the first part.

14. (Previously presented - withdrawn) A fabricating method as claimed in claim 12, wherein the forming N-well is carried out by selectively implanting phosphorus ions into a part of the second region that becomes the second part.

15. (Previously presented - withdrawn) A fabrication method as claimed in claim 3, wherein the forming the isolation region is carried out in LOCOS (Local Oxidation on Substrate) process.

16. (Previously presented - withdrawn) A fabricating method as claimed in claim 3, wherein the forming the isolation region is carried out in STI (Shallow Trench Isolation) process.

17. (Previously presented - withdrawn) A fabricating method as claimed in claim 3, wherein the simultaneously growing oxide films is carried out in single thermal oxidation process.

18. (Previously presented - withdrawn) The method of claim 3, wherein the second and third MOSFETs have equal gate-channel leakage current characteristics.

19. (Previously amended - withdrawn) The method of claim 18, wherein the standby current in each of the second and third MOSFETs depends on subthreshold characteristics, said subthreshold characteristics comprising other than gate channel leaking current characteristics.

Claim 20. (New) A semiconductor device comprising:

a first MOSFET having a first gate oxide film;

a second MOSFET of an n-type having a threshold level which is relatively higher than said first MOSFET, the second MOSFET having a second gate oxide film thicker than the first gate oxide film; and

a third MOSFET of a p-type having a threshold level which is relatively higher than said first MOSFET, the third MOSFET having a third gate oxide film which is thicker than

the first gate oxide film and is thinner than the second gate oxide film, wherein said second MOSFET and said third MOSFET form a single CMOS pair.